In the Claims

Amend the claims as follows:

1. (currently amended) A semiconductor device comprising:

a first interconnect adjacent a second interconnect on an interconnect level;

beneath at least one of the first and second interconnects, an etch stop layer positioned over an underlying via insulator level;

spacers formed along adjacent sides of the first and second interconnects; and

an air gap formed between the first and second interconnects, the air gap extending above an upper surface of at least one of the first and second interconnects and the air gap extending below a lower surface of the at least one of the first and second interconnects having the etch stop layer beneath by a distance corresponding to a thickness of the etch stop layer, distance between the spacers defining the width of the air gap.

2. (original) The semiconductor device of claim 1 wherein the air gap is self-aligned to the adjacent sides of the first and second interconnects.

3. (original) The semiconductor device of claim 1 wherein the spacers adjacent the sides of the first and second interconnects comprise silicon dioxide or silicon nitride.

4. (cancelled)

5. (original) The semiconductor device of claim 4 wherein the etch stop layer comprises silicon carbide.

6. (original) The semiconductor device of claim 4 wherein the underlying via insulator level comprises silicon dioxide or fluorinated silicon dioxide.

7. (previously presented) The semiconductor device of claim 1 further including hardmask spacers self-aligned to either side of an upper portion of the air gap, wherein the air gap extends between and below the hardmask spacers.

8. (original) The semiconductor device of claim 7 wherein the hardmask spacers comprise silicon dioxide or silicon nitride.

9. (original) The semiconductor device of claim 1 further including at least one insulative layer above the interconnect level and the air gap, and wherein the air gap extends into the insulative layer.

10. (original) The semiconductor device of claim 9 wherein the at least one insulative layer above the interconnect level and the air gap comprises silicon nitride or silicon carbon nitride as a capping layer for the interconnect and silicon dioxide or fluorinated silicon dioxide as an insulative layer above the capping layer.

11. (original) The semiconductor device of claim 1 further including hardmask spacers self-aligned to either side of an upper portion of the air gap, and an insulative

layer above the interconnect level, the air gap and the hardmask spacers, and wherein the air gap extends between the hardmask spacers and upward into the insulative layer.

12. (original) The semiconductor device of claim 1, wherein the first and second interconnects are formed by a damascene or dual damascene process.

13. (original) The semiconductor device of claim 1, wherein the first and second interconnects comprise copper, aluminum, tungsten or gold.

14. (original) The semiconductor device of claim 1 further including, beneath one of the first and second interconnects, an etch stop layer positioned over at least one underlying via insulator level, and below the underlying via insulator, a second interconnect level.

15. (original) The semiconductor device of claim 14 further including, between the at least one underlying via insulator level and the second interconnect level, a selective metal deposition layer comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer.

16. (original) The semiconductor device of claim 1 further including, over each of the first and second interconnects, a selective metal deposition layer comprising a selective tungsten layer or a selective cobalt tungsten phosphide layer.

17-20. (cancelled)